

CLAIMS

1. A method for forming a contact over a silicide layer situated in a semiconductor die, said method comprising steps of:  
depositing a barrier layer on sidewalls of a contact hole and on a native oxide  
5 layer situated at a bottom of said contact hole, said sidewalls being defined by said contact hole in a dielectric layer;  
removing a portion of said barrier layer and said native oxide layer situated at said bottom of said contact hole to expose said silicide layer.

10 2. The method of claim 1 wherein said step of removing said portion of said barrier layer and said native oxide layer situated at said bottom of said contact hole comprises utilizing a sputter etch process.

15 3. The method of claim 1 wherein said dielectric layer comprises top corner regions situated adjacent to said contact hole, wherein said top corner regions of said dielectric layer are not etched during said step of removing said portion of said barrier layer and said native oxide layer situated at said bottom of said contact hole.

20 4. The method of claim 1 wherein said step of depositing said barrier layer on said sidewalls of said contact hole is optimized such that said barrier layer has a greater thickness at a top of said contact hole than a thickness at a bottom of said contact hole.

5. The method of claim 2 wherein said contact hole has an electrical contact width, wherein said electrical contact width is not increased by said sputter etch process.

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6. The method of claim 1 wherein said barrier layer comprises titanium/titanium nitride.

7. The method of claim 1 wherein said dielectric layer comprises PECVD  
10 oxide.

8. A method for forming a contact over a silicide layer situated in a semiconductor die, said method comprising steps of:

removing a native oxide layer situated over said silicide layer at a bottom of a  
15 contact hole by utilizing a reactive hydrogen pre-clean process, said sidewalls being defined by said contact hole in a dielectric layer, said dielectric layer having top corner regions situated adjacent to said contact hole;

depositing a barrier layer on said sidewalls of said contact hole and over said silicide layer.

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9. The method of claim 8 wherein said reactive hydrogen pre-clean process does not etch said top corners of said dielectric layer.

10. The method of claim 8 wherein said contact hole has an electrical contact width, wherein said electrical contact width is not increased by said reactive hydrogen pre-clean process.

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11. The method of claim 8 wherein said dielectric layer comprises PECVD oxide.

12. The method of claim 8 wherein said barrier layer comprises  
10 titanium/titanium nitride.

13. The method of claim 8 wherein said native oxide layer comprises thermally grown oxide.

15 14. A method for forming a contact over a silicide layer situated in a semiconductor die, said method comprising steps of:

depositing a barrier layer on sidewalls of a contact hole and on a native oxide layer situated at a bottom of said contact hole, said sidewalls being defined by said contact hole in a dielectric layer, said native oxide layer being situated over said  
20 silicide layer;

removing said native oxide layer situated over said silicide layer at said bottom of said contact hole by utilizing a sputter etch/deposition process.

15. The method of claim 14 wherein said step of removing said native oxide layer situated over said silicide layer at said bottom of said contact hole comprises simultaneously sputter etching said barrier layer and said native oxide layer and  
5 depositing titanium/titanium nitride on said barrier layer.

16. The method of claim 14 wherein said sputter etch/deposition process has a sputter etch/deposition ratio greater than 1.0.

10 17. The method of claim 14 wherein said dielectric layer comprises top corner regions situated adjacent to said contact hole, wherein said sputter etch/deposition process does not etch said top corner regions of said dielectric layer.

18. The method of claim 14 wherein said contact hole has an electrical  
15 contact width, wherein said electrical contact width is not increased by said sputter etch/deposition process.

19. The method of claim 14 wherein said sputter etch/deposition process comprises an argon sputter etch.

20 20. The method of claim 14 wherein said dielectric layer comprises PECVD oxide.